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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/022,364	12/20/2001	Francis J. Kub	N.C. 79,684	3513

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NAVAL RESEARCH LABORATORY
ASSOCIATE COUNSEL (PATENTS)
CODE 1008.2
4555 OVERLOOK AVENUE, S.W.
WASHINGTON, DC 20375-5320

EXAMINER	
FOURSON III, GEORGE R	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 11/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/022,364	KUB ET AL.	
	Examiner	Art Unit	
	George Fourson	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 10-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 10-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 8/28/06 has been entered.

Claims 1-8 are objected to because of the following informalities: In claims 1-8, the use of "single crystal semiconducting material" as opposed to "single crystal semiconductor material" is incorrect because it implies use of the material. Also, claim 8 recites "semiconductor material" which is inconsistent with the language of claim 1 for example. Appropriate correction is required.

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 1-4 and 7 are rejected under 35 U.S.C. 102(b) as being anticipated by Henley et al 6013567.

Henley et al. (' 567) teaches a method of forming thin film material on a device which includes providing silicon wafer 2100 (Col. 12, lines 20-22 and Col. 16, lines 34-39), then forming thin film 2101 on silicon wafer 2100 (Col. 12, lines 22-25, Col. 3, lines 56-60, and Fig. 12), then optionally forming stiffening layer 2102 on surface of silicon wafer 2100 (Col. 12, lines 28-30), subsequently implanting hydrogen at selected depth (Zo) into silicon wafer 2100 wherein during a portion of the implanting step the stiffening material is implant damaged as in the instant invention thereby forming hydrogen ion layer 2111 (Col. 4, lines 53-55, and Col. 12, lines 34-38

and 56-65), then optionally applying an adhesive layer between bonding surfaces of silicon wafer 2100 and flexible substrate 2201 (Col. 13, lines 32-34), subsequently bonding silicon wafer 2100 to flexible substrate 2201 such as plastic (Col. 12, line 66 to Col. 13, line 6, and Fig. 13), subsequently splitting silicon wafer 2100 along hydrogen ion layer 2111 by using liquid or gas jet directed at the side of silicon wafer 2100 (Col. 14, line 64 to Col. 15, line 9), and then smoothing surface 2601 of the resulting silicon wafer 2100 (Col. 15, line 66 to Col. 16, line 10, and Fig. 17).

Applicant argues that the substrate 2201 of Henley et al '567 is disclosed at col.13, line 55 to be silicon. However, at column 13, line 5, substrate 2201 is disclosed to be plastic.

Claims 5,6 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Henley et al '567 as applied to claims 1-4 and 7 above, and further in view of Goesele et al 5877070 and Thilderkvist et al 6489241.

Henley et al '567 does not disclose implantation of boron in addition to implanting hydrogen or directing nitrogen gas stream or liquid stream to split the substrate along the implanted layer.

Goesele et al '070 discloses a process of bonding a substrate comprising hydrogen implanted layer to another substrate followed by cleaving wherein boron is implanted in addition to hydrogen to produce hydrogen traps (col.9, lines 57-65).

Thilderkvist et al '241 discloses a process of bonding a substrate comprising hydrogen implanted layer to another substrate followed by cleaving wherein separation is performed by directing a nitrogen gas stream to the edge of the bonded assembly (col.12, lines 14 and 16).

It would have been within the scope of one of ordinary skill in the art to combine the teachings of Henley et al '567 and those of Goesele et al '070 and Thilderkvist et al '241 to enable the step of implantating species to induce splitting and the step of splitting/cleaving of Henley et al '567 to be performed according to the teachings of Goesele et al and Thilderkvist et al because one of ordinary skill in the art would have been motivated to look to analogous art teaching alternative suitable or useful methods of performing the disclosed implanting and cleaving steps of Henley et al '567 and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

Claims 10-13,15,16, 18-19 and 22-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Henley et al. ('567) as applied to claims 1-4 and 7 above, and further in view of Lutzen et al. (' 169).

Henley et al. does not disclose the steps recited in claim 10, lines 2-8.

Lutzen et al. discloses a method of forming a semiconductor device which includes providing substrate W 1 (Paragraph [0041], and Fig. 1A), then forming oxide layer 2A consisting of material such as semiconductor layer, electrically conductive layer and dielectrics such as metal oxides on substrate W1 (Paragraph [0041] and [0045]), then forming adhesion and barrier layer 2B consisting of more than one conductive layer including titanium, platinum and iridium (Paragraphs [0041], [0008], [0045]), subsequently forming another thin film layer 2A consisting of material such as semiconductor layer, electrically conductive layer and dielectrics such as metal oxides (Paragraph [0041] and [0045]), subsequently bonding substrate W2 with hydrogen ion implant to substrate WI (Paragraph [0042], and Fig. 1B), and then splitting substrate W2 (Paragraph [0044], and Fig. 1C).

It would have been within the scope to one ordinary skill in the art to combine both teachings because it would enable formation protective layer 2A and 2B of Lutzen et al in the process of Henley et al. and enable the advantage of preventing incompatible materials from diffusing out via the necessary connecting paths thus making it possible to prevent negative mutual influences between the elements in the various element layers during production process or in operation (Paragraph [0029]).

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Henley et al '567 in view of Lutzen as applied to claim 10 above, and further in view of Thilderkvist et al.

Thilderkvist et al is applied as above in providing motivation to perform the cleaving process of Henley et al '567 by directing nitrogen gas at the side of the bonded construction of Henley et al '567.

Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Henley et al '567 in view of Lutzen as applied to claim 10 above, and further in view of Lee et al 6312567.

With respect to claim 17, the combination process does not disclose that the protective layer is comprised of MgO.

Lee et al. dicloses the use of MgO as a dielectric material for use in semiconductor fabrication process and as an alternative to silicon dioxide for use in semiconductor fabrication process (Col. 4, lines 49-51).

It would have been within the scope to one ordinary skill in the art to combine the teachings of Lee et al. with the combination process because it would enable formation of the dielectric layer 2A of Henley to be performed.

Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Henley et al in view of Lutzen et al as applied to claim 10 above, and further in view of Goesele et al '070.

Goesele et al '070 is relied on as stated above as providing motivation to include a co-implant of B in the process of implanting a species to induce splitting in the process of Henley et al '567.

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Henley et al. ('567) in view of Lutzen et al. '169 as applied to claim 10 above and further in view of Srikrishnan ('987).

The combination process does not teach the step as recited in claim 20.

Srikrishnan teaches a method of forming a thin film on a semiconductor device which includes providing a single crystalline semiconductor substrate 500 (Col. 4, lines 22-23, and Fig.5A), then forming etch stop layer 505 comprised of material such as Si-Ge or Ge (Col. 4, lines 28-38), subsequently forming thin device layer 510 over substrate 500 (Col. 4, lines 43-45), subsequently forming stiffening layer 515 (Col. 4, lines 56-57, and Fig. 5B), then implanting hydrogen ions into substrate 500 thereby forming hydrogen ion layer 502 (Col. 5, lines 4-10, and Fig. 5B), subsequently bonding substrate 500 with substrate 530 (Col. 5, lines 25-26, and Fig.5C), then splitting substrate 500 at the hydrogen ion layer 502 (Col. 5, lines 33-36, and Fig. 5D), then

annealing device layer 510' in order to promote a stronger bonding between substrate 530 and device layer 510' (Col. 5, lines 46-50).

It would have been within the scope to one ordinary skill in the art to combine the teachings of Srikrishnan with the combination because it would enable the step of annealing thin film 2101 of the combination to be performed and obtain further advantage of promoting a stronger bonding between substrate 530 and device layer 510' (Srikrishnan, Col. 5, lines 46-50).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to George Fourson whose telephone number is (571) 272-1860. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith, can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

George Fourson
Primary Examiner
Art Unit 2823

GFourson
November 3, 2006